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A new 0.8µm CMOS image sensor with low RTS noise and high full well capacity

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***Abstract*—**This is a report of a new 0.8µm, 32 mega pixel CMOS image sensor (CIS) with OmniVision second-generation (Gen2) stacking technology. In this work, we re-designed a pixel layout and developed a vertical transfer gate (VTG) to achieve low noise and high full well capacity (FWC). The sensor achieved a total read noise of 1.2e- rms and a linear FWC of 5000e-. The random telegraph signal (RTS) noise was reduced 70% compared with that of a 0.9µm pixel. Other pixel performance improvements are also realized in this work.

I. INTRODUCTION

Image quality of smartphone cameras has recently been evolving with dual camera applications [1]. For example, the dual camera enhances low light image quality and can have an optical zoom function. Additionally, high resolution image sensors have attracted attention to complementing a zoomed image in the dual camera. For this reason, the demand of high resolution image sensors in mobile markets has increased, and the pixel size shrinkage has accelerated into submicron pixel regime [2,3].

In the past, many pixel technologies have been developed to improve pixel performance degradations caused by pixel size reduction. Specifically, backside illumination (BSI) technology reduces photo sensitivity loss by collecting light from the sensor backside [4]. Backside deep trench isolation (BDTI) and composite metal-oxide grid (CMG) technologies improve SNR10 [5] by suppressing optical crosstalk with physical isolations [6,7]. Moreover, stacking technology contributes not only to reducing chip size but also to improving dark characteristics, such as noise and white pixels, by optimizing the sensor process independently.

In addition to these performance improvements, noise and FWC are key characteristics for submicron pixels. As is well known, sizes of source follower (SF) transistor and photo diode (PD) are important factors for noise and FWC. However, their sizes become extremely small in submicron pixels according to the conventional shrink methodology. In this paper, we present a new 0.8µm pixel that addresses the noise and FWC issues.

II. PIXEL ARCHITECTURE

Figure 1 shows a schematic diagram of the 0.8µm pixel. The pixel array size is 32 mega (6528(H)x4896(V)), and a standard 2x2 shared pixel architecture is adopted in this work. Regarding the process technology, the OmniVision Gen2 stacking technology is continuously used for the 0.8µm pixel; same as the 0.9µm pixel. As shown in Fig. 2, the logic wafer and the CMOS image sensor (CIS) wafer are connected at the column level using wafer-to-wafer bonding technology. The BDTI and the CMG are also used to achieve a good optical performance. In addition to the Gen2 stacking technology, a 40nm process node is newly adopted in CIS metal layers to correspond to pixel size reduction. As a result, all necessary metal lines are prepared in a 2x2 pixel layout. The 40nm process node also helps to suppress a metal-to-metal coupling, such as floating diffusion (FD) to adjacent bit-line, which causes an electrical crosstalk, while current process can't suppress it due to the layout limitation.

As mentioned above, the challenge in submicron pixels is noise and FWC. They also have trade off relationship since SF transistor and shallow PD regions can't overlap each other to avoid the leakage between them (Fig. 3). Therefore, in a conventional pixel design, both SF and PD areas can't be enlarged at the same time. In other words, it is difficult to prevent both noise and FWC from degrading due to the pixel size shrinkage by using the conventional pixel design. In order to overcome this issue, we developed a VTG technology and a re-designed pixel layout.

Pixel structures of a conventional and VTG pixel are compared in Fig. 3 with potential profiles. In case of the conventional pixel, a pinning voltage (Vpin), which is a maximum potential of a PD, should be kept in a shallow region considering a complete charge transfer from PD to FD. Therefore, the shallow PD area and doping concentration are important parameters to achieve higher FWC. On the other hand, the VTG can read out charged

electrons from deeper region compared with a conventional transfer gate (TX), thus the Vpin can be shifted to a deep PD region that has larger PD area. Consequently, FWC can be increased. This is the advantage of the VTG pixel. Fig. 4 shows PD potential profiles confirmed by TCAD device simulations. It is clearly seen that the Vpin of the VTG pixel is shifted from shallow to deep position. Besides the VTG, higher energy implantation is introduced to increase PD capacitance of the backside region, enhancing FWC. Both implant layout and dosage condition are well optimized in TCAD simulations to achieve no lag, no blooming and high FWC for the VTG pixel.

Owing to the VTG pixel structure, flexibility of a pixel transistor layout is increased because there is no shallow PD in the VTG pixel. Hence, we re-designed the pixel transistor layout. Fig. 5 shows schematics of a conventional and new pixel layout. Pixel transistors are separated into horizontal and vertical direction in the new layout, whereas the conventional layout has only horizontal pixel transistors. The new layout has the advantage of maximizing the SF transistor area while keeping length of other transistors. As shown in Fig. 6, SF transistor area is increased 75% compared with that of the conventional layout. The new layout also enables us to minimize the transistor width of vertical direction, thus RST clock feed through is minimized despite of SF area increasing. Furthermore, as shown in Fig. 7, it is possible to have an additional transistor in vertical direction for extended function, for instance, FD binning and dual conversion gain.

III. EXPERIMENTAL RESULT

The measured noise histogram comparing the 0.9μm and 0.8μm pixel is shown in Fig. 8. As clearly seen, the RTS noise [8] of the 0.8μm pixel is significantly suppressed compared with that of the 0.9μm pixel. The read noise for the 0.8μm pixel at 16x analog gain is 1.2e-rms. It is also decreased compared with that of the 0.9μm. Figure 9 shows FWC result normalized to a 1.0μm pixel. The linear FWC of the 0.8μm pixel (Red circle) is 5000e-, which is 20% larger than estimated value based on the conventional pixel design (Blue circle). This is the same level of FWC as the 0.9μm pixel. Consequently, both noise and FWC, which have trade-off relationship, are greatly enhanced with the new layout and VTG pixel.

Figure 10 shows results of VTG process dependence. The left figure shows VTG depth dependence of the black dots, which is one of the lag characteristic. The black dots are decreased, which means the lag is improved, by increasing the VTG depth. The right figure shows blooming characteristic with different VTG layouts. The blooming of the layout “B” is reduced 90% compared with that of the layout “A”. These results indicate that the optimized VTG process improves the potential profile around VTG in terms of charge transfer and anti-blooming characteristic. As a result, no lag and no blooming are achieved.

The quantum efficiency (QE) curve is measured and compared with that of the 0.9μm pixel, as shown in Fig.11. The optical crosstalk of the 0.8μm pixel is suppressed, similar to the 0.9μm one. The QE peak degradation is also minimized while the sensitivity is decreased 24% due to the pixel size shrinkage. Both optical characteristics are attributed to adjusting the CMG width in addition to the BDTI. Figure 12 shows a sample color image that is taken with the 0.8μm pixel.

IV. CONCLUSION

A novel 0.8μm pixel CMOS image sensor with the new layout and VTG structure is demonstrated. The summary of pixel performance comparing the 0.9μm and 0.8μm pixel is listed in table 1. The 0.8μm pixel achieves a RTS noise of 8ppm, which is a 70% reduction compared to that of the 0.9μm pixel, and a FWC of 5000e-, which is the same level as the 0.9μm pixel, in spite of the pixel size reduction. A read noise of 1.2e-rms is achieved and good optical performance is obtained. This technology is used in the 0.8μm, 32 mega pixel CIS product and is extended to a 48 mega pixel CIS product.

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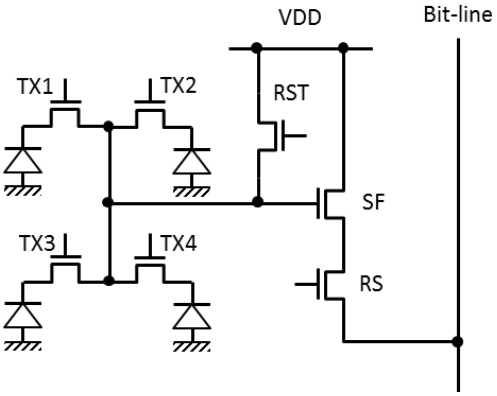


Fig. 1: Schematic diagram of the 0.8μm pixel.

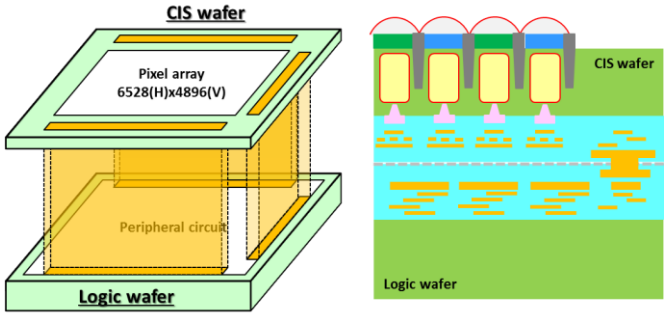


Fig. 2: Block diagram and schematic of the 0.8μm pixel.

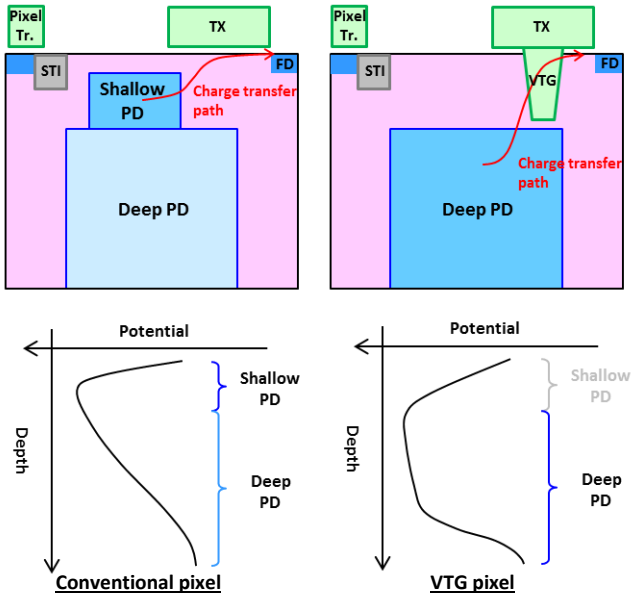


Fig. 3: Schematics of conventional pixel and VTG pixel with potential profiles.

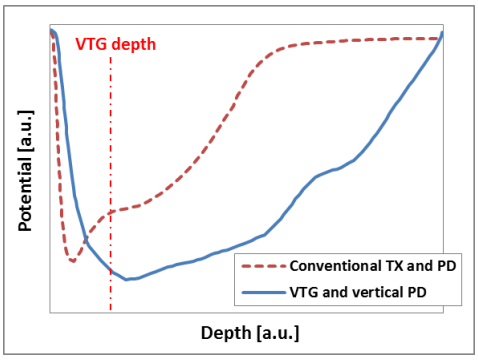


Fig. 4: Potential profiles of photo diode based on the TCAD simulation results.

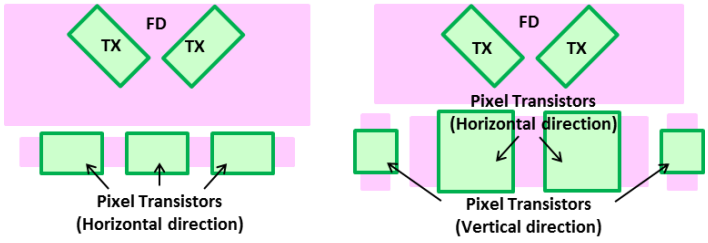


Fig. 5: Conventional pixel layout and new pixel layout.

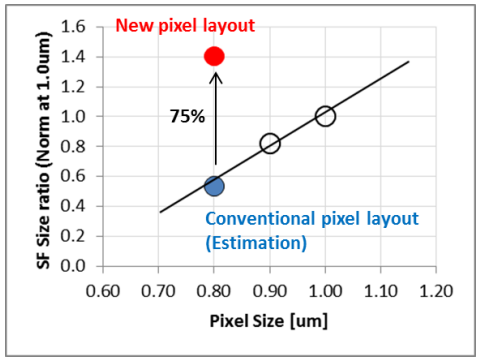


Fig. 6: Pixel size dependence of SF transistor area.

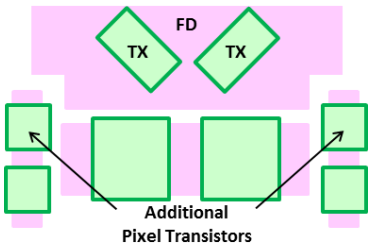


Fig. 7: Extended pixel layout with additional transistor.

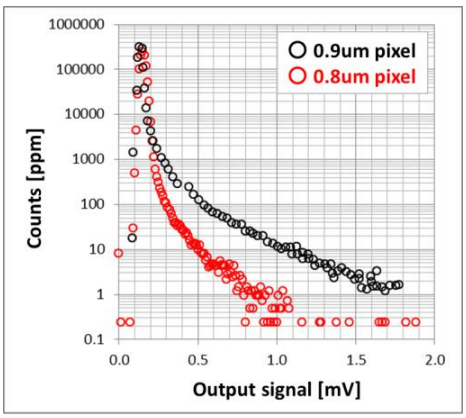


Fig. 8: Measured noise histogram comparing the 0.9µm and 0.8µm pixel.

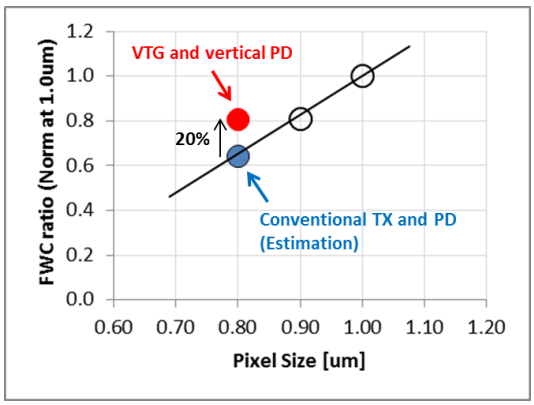
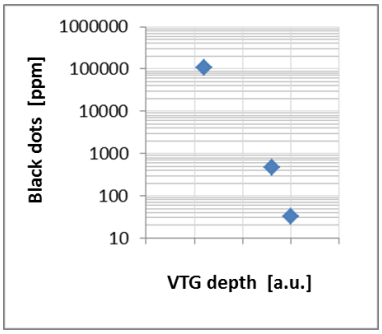
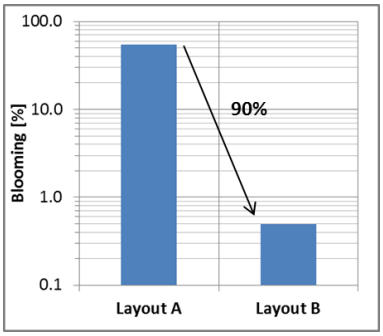


Fig. 9: Pixel size dependence of measured FWC.



VTG depth dependence of black dots



VTG layout dependence of blooming

Fig. 10: VTG process optimization results.

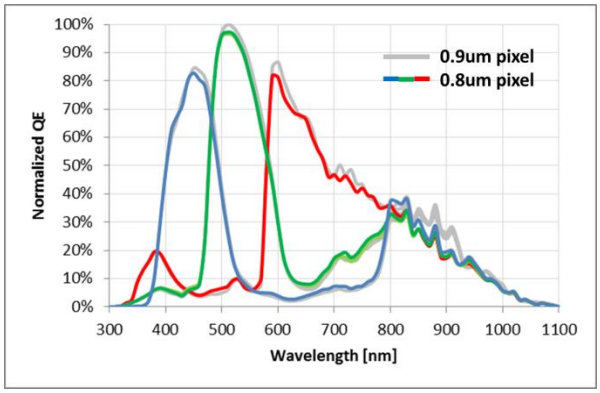


Fig. 11: Quantum efficiency curve comparing the 0.9µm and 0.8µm pixel

Fig. 12: Sample image of the 0.8µm pixel

Parameter	Units	0.9um pixel	0.8um pixel
Linear Full well capacity	e-	5000	5000
Sensitivity – G (530nm)	e-/lux.sec	2645	2010
SNR10	lux	103	115
Read noise (16x gain)	e-	1.5	1.2
RTS (>1mV)	ppm	30	8
Blooming	%	<1	<1
Lag	e-	<1	<1
Dark current (Tj=60°C)	e-/sec	2.3	2.2

Table 1: Measured pixel performances for the 0.9µm and 0.8µm pixel.